Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A display drive circuit comprising:

Random Access Memory which sequentially stores data for image display that is input continuously;

a plurality of grayscale pattern selection circuits, each selecting one grayscale pattern from a plurality of grayscale patterns, based on data stored in the Random Access Memory, the Random Access Memory is electrically connected to the plurality of gray scale pattern selection circuits; and

a plurality of frame selection circuits which are provided in correspondence with the plurality of grayscale pattern selection circuits, and sequentially output grayscale patterns selected by the plurality of grayscale pattern selection circuits for a series of image frames.

2. (Previously Presented) The display drive circuit as defined in claim 1, further comprising:

an image data conversion circuit which receives data in which grayscales are represented by N bits (where N is an integer greater than or equal to 2), converts the received data into data in which grayscales are represented by M bits (where M is an integer such that $M > N$), based on a set command, and supplies the converted data to the Random Access Memory.

3. (Currently Amended) The display drive circuit as defined in claim 1, wherein each of the plurality of grayscale pattern selection circuits includes:

a selection Read Only Memory which outputs a grayscale pattern selection signal based on data stored in the Random Access Memory; and

~~an~~a Frame Rate Control Read Only Memory which selects one grayscale pattern from among the plurality of grayscale patterns in accordance with the outputted grayscale pattern selection signal, and uses the selected grayscale pattern to perform frame rate control (FRC) modulation in accordance with a control signal that is output from the corresponding frame selection circuit.

4. (Currently Amended) The display drive circuit as defined in claim 2, wherein each of the plurality of grayscale pattern selection circuits includes:

a selection Read Only Memory which outputs a grayscale pattern selection signal based on data stored in the Random Access Memory; and

~~an~~a Frame Rate Control Read Only Memory which selects one grayscale pattern from among the plurality of grayscale patterns in accordance with the outputted grayscale pattern selection signal, and uses the selected grayscale pattern to perform frame rate control (FRC) modulation in accordance with a control signal that is output from the corresponding frame selection circuit.

5. (Original) The display drive circuit as defined in claim 1,

wherein each of the frame selection circuits is divided into a plurality of portions that are disposed on either side of the corresponding grayscale pattern selection circuit.

6. (Currently Amended) A display drive circuit comprising:

Random Access Memory which sequentially stores data for image display that is input continuously;

a plurality of Frame Rate Control Read Only Memory which store a plurality of grayscale patterns with mutually different frame cycles, and use data stored in the Random Access Memory to select one grayscale pattern from among the plurality of grayscale patterns; and

a plurality of frame selection circuits each of which sequentially outputs the selected grayscale pattern selected by the Frame Rate Control Read Only Memory, for each frame,

wherein a drive signal for driving a display portion is output based on the outputted grayscale pattern from the Frame Rate Control Read Only Memory;

and the Random Access Memory is electrically connected ~~to the each of the plurality of Frame Rate Control Read Only Memory.~~ a plurality of grayscale pattern selection circuits.

7. (Previously Presented) The display drive circuit as defined in claim 6, further comprising:

an image data conversion circuit which receives data in which grayscales are represented by N bits (where N is an integer greater than or equal to 2), converts the received data into data in which grayscales are represented by M bits (where M is an arbitrarily settable integer such that M > N), and supplies the converted data to the Random Access Memory,

wherein each of the frame selection circuits outputs the selected grayscale pattern based on the M-bit grayscales, for each frame.

8. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 1; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

9. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 2; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

10. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 3; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

11. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 4; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

12. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 5; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

13. (Original) A semiconductor integrated circuit comprising:

the display drive circuit as defined in claim 6; and

a terminal which outputs a drive signal generated on the basis of the selected grayscale pattern.

14. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 1, which drives the segment electrodes.

15. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 2, which drives the segment electrodes.

16. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 3, which drives the segment electrodes.

17. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 4, which drives the segment electrodes.

18. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 5, which drives the segment electrodes.

19. (Original) A display panel comprising:

pixels specified by a plurality of common electrodes and a plurality of segment electrodes, which mutually intersect; and

the display drive circuit as defined in claim 6, which drives the segment electrodes.

20. (Original) A display drive method comprising:

selecting one grayscale pattern from among a plurality of grayscale patterns having at least two types of frame cycles, based on data for image display, and outputting the selected grayscale pattern for each frame; and

outputting a drive signal for driving a display portion, based on the selected grayscale pattern.

21. (Original) The display drive method as defined in claim 20,

converting grayscales of N bits (where N is an integer greater than or equal to 2) into grayscales of M bits (where M is an arbitrarily settable integer such that $M > N$); and

selecting one grayscale pattern from among the plurality of grayscale patterns having at least two types of frame cycles, based on the M-bit grayscales, and outputting the selected grayscale pattern for each frame.

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22. (Currently Amended) A display drive circuit which drives a display panel having a plurality of common electrodes and a plurality of segment electrodes, the display drive circuit comprising:

a Random Access Memory which stores data for image display;

a plurality of Frame Rate Control Read Only Memories which store a plurality of grayscale patterns with mutually different frame cycles;

a grayscale pattern selection circuit which selects one Frame Rate Control Read Only Memory from among the plurality of Frame Rate Control Read Only Memories, based on data stored in the Random Access Memory, the Random Access Memory is electrically connected to the grayscale pattern selection circuit;

a frame selection circuit which outputs an address signal indicating a frame number; and

a segment electrode drive circuit which outputs a drive signal to one of the plurality of the segment electrodes, the drive signal corresponding to a result of a computation using an orthogonal function which is specified by a scan pattern for four lines of common electrodes selected simultaneously by a multi-line drive method,

each of the plurality of the grayscale patterns being a pattern indicating display on/off for one dot of each frame for frame cycles,

the Frame Rate Control Read Only Memory outputting a signal indicating display on/off of a frame specified by the address signal, the Frame Rate Control Read Only Memory being selected by the grayscale pattern selection circuit,

the segment electrode drive circuit using the signal indicating display on/off for the computation using the orthogonal function.

23. (Previously Presented) The display drive circuit as defined in claim 22, the signal indicating the display on/off being outputted to the segment electrode drive circuit from the Frame Rate Control Read Only Memory, the outputted signal being shared by one of odd-numbered lines and even-numbered lines of the common electrode selected simultaneously.

24. (Previously Presented) The display drive circuit as defined in claim 22, further comprising:

first to third latch circuits which latch a plurality of bits for each color, based on first to third write control signals; and

fourth to sixth latch circuits which latch outputs of the first to third latch circuits, based on a write delay control signal which is delayed in relation to the third write control signal,

the first to third write control signals going active in sequence every time a given write control signal becomes active, and

outputs of the fourth to sixth latch circuits being supplied to the Random Access Memory.

25. (Previously Presented) The display drive circuit as defined in claim 22, the frame selection circuit being divided into portions each of which is disposed on either side of the corresponding grayscale pattern selection circuit.

26. (Previously Presented) A display panel, comprising:

a plurality of common electrodes;

a plurality of segment electrodes;

a plurality of pixels; and

the display drive circuit as defined in claim 22, which drives the segment electrodes.